29.5 A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor

Toshihiro Hattori[1], Takahiro Irita[1], Masayuki Ito[1], Eiji Yamamoto[1], Hisashi Kato[1], Go Sado[1], Tetsuhiro Yamada[1], Kunihiko Nishiyama[1], Hiroshi Yagi[1], Takao Koike[1], Yoshihiko Tsuchihashi[1], Motoki Higashida[1], Hiroyuki Asano[1], Izumi Hayashibara[1], Ken Tatezawa[1], Yasuhisa Shimazaki[1], Naozumi Morino[1], Kenji Hirose[1], Saneaki Tamaki[1], Shinichi Yoshioka[1], Reiko Tsuchihashi[2], Nobuto Arai[2], Tomohiro Akiyama[2], Koji Ohno[2]

[1]Renesas Technology, Tokyo, Japan
[2]NTT DoCoMo, Tokyo, Japan

Presently, cellular phones are used not only for voice communications, e-mail, and web browsing, but also for more advanced functions such as video telephony and 3D Java games. Therefore, a high performance application processor, for example SH-Mobile[1], is typically embedded in a cellular phone in addition to the baseband processor. In the baseband processor, dual mode operation is required supporting both the high-performance WCDMA service and the GSM/GPRS service which is generally available worldwide. Therefore, present cellular phone handsets are implemented by mounting two or three processors, which manage their power activity in each usage case to maximize battery life. Though a single chip integration of application and baseband processor(s) is obviously attractive, a novel scheme which can control the power inside the chip is required to realize the integration.

Figure 29.5.1 shows a block diagram of the chip. In the chip, 3 domains are defined. Each domain has a CPU, which runs a different OS. Therefore, this system architecture runs multiple OS's on heterogeneous multi-CPU cores. The major reason why we designed a 3-domain architecture in the chip is to: (1) maximize the reuse of huge software assets of conventional cellular phones by keeping the same system architecture, (2) enable separate system development in cellular phone design, (3) introduce different efficient power shut down schemes according to the cellular phone use for the reduction of leakage power consumption, (4) reduce the conflicts between each subsystems, and (5) support separate dynamic clock frequency changes for each domain for the reduction of dynamic power consumption.

Figure 29.5.2 indicates our concept of "power domains" separating the chip into 20 by functionality and characteristics. Domains A1A, A1R, A2, A3, AC, A4U1, A4U2 and A4 take roles of application processors and domains BA3, BA4, BW1, BW2, BW3, BG1, BG2, BG3 and BC do that of baseband processors respectively.

BW1, BW2 and BW3 contain DSP and accelerators for the WCDMA protocol; BG1, BG2 and BG3 contain DSP and accelerators for GSM/GPRS protocol. While waiting for a call, BW3 and BG3 are kept powered to trace the timing of each radio; BW2, BW1 and BG2, BG1 will be powered on at appropriate timing for paging activities. If a call comes, they will interrupt the ARM926EJ-S processor residing in BA3 which handles WCDMA and GSM protocol stacks. Note that BW1-BW3 or BG1-BG3 can be cut off completely in such environments where only one protocol is available.

Domain A1A contains an ARM926EJ-S core and A1R contains an SH-X2 core. A general purpose OS runs on the former and a real-time OS runs on the latter. Because these cores need higher performance, they are designed to achieve a high operating frequency of up to 208MHz and 312MHz, respectively, by utilizing a higher proportion of low threshold (high leakage) transistors, whereas the other domains are designed with a restricted proportion of such transistors. Therefore, these cores are assigned to individual power domains to be able to cut off the power according to usage.

A4U1 and A4U2 that contain VRAM and a LCD controller are designed specifically to realize low power LCD refresh functionality. Figure 29.5.2 focuses on the activation of each power domain in this case. The clock source can be changed to the VCTCXO input so as to keep refreshing even after all PLL and oscillators for the application part are turned off. An additional 10mW, including I/O, was measured in sustaining the refresh operation at 56Hz.

The deepest level of power off is called "Ultra Stand-by mode", in which all domains except for C5 can be powered off in the case that the power switch of the handset is off. As described, the power state of the chip can be programmed flexibly on a case-by-case basis considering the trade-offs between leakage current and time to recovery.

Problems that occur by increasing the number of power domains are: (1) routing problems of global nets and clock trees, (2) integrity of shutdown elements that should be inserted between power domains and (3) stability of VDD/GND lines of active domains while transitions of the power state of the other domains.

The domain C4 is introduced to avoid problem (1). This domain is shaped like slits with proper spacing and defined as a mostly powered on domain. Introducing this concept [2], we can place repeaters to transmit global nets and buffers consisting clock trees by utilizing C4 area as stepping-stones.

Addressing problem (2), signals from a domain which may be powered off should be transmitted through special circuits called μI/O [3]. To minimize the overhead of inserting μI/Os, we adopt a hierarchical power domain structure [2]. There is some relationship between each power domain in terms of their functionality. Exploiting such relationships, we defined a hierarchical relation between power domains as shown in Fig. 29.5.3. The μI/Os on the nets from higher to lower hierarchy can be omitted because a higher domain will not be powered off while a lower one is powered on.

To resolve problem (3), a power switch design was developed to minimize rush current [2] and a sequential power on scheme was established. When SYSC processes a power-on request for several domains, it issues the power-on signal to the corresponding power switches one-by-one and waits for the ready signal from it. This logic is designed as domino-logic, which establishes minimum wakeup time satisfying VCC/GND stability.

Figure 29.5.4 shows some examples of activating power domain in scenes of mobile phone usage. Figure 29.5.5 shows the measurement results of leakage current in several usage cases. Case 2 corresponds to a handset waiting for a call; a leakage current of 299 μA @rt is achieved. Figure 29.5.6 shows the domain partition on the chip. The chip is fabricated in a 90nm, 8M(7Cu+1Al), CMOS dual-Vth low-power process technology. The die size is 11.15×11.15mm^2 and a chip micrograph is shown in Figure 29.5.7. Supply voltages are 1.2V(internal) and 1.8/2.5/3.3V(I/O). It integrates a total of 181M transistors, 13.5M logic gates and 20.2Mb memory.

References:

[1] T. Kamei, et al., "A Resume-Standby Application Processor for 3G Cellular Phones," *ISSCC Dig. Tech. Papers*, pp. 336-337, Feb., 2004.
[2].Y. Kanno, et al., "Hierarchical Power Distribution with 20 Power Domains in 90nm Low-Power Multi-CPU Processor," *ISSCC Dig. Tech. Papers*, Paper 29.4, Feb., 2006
[3] Y. Kanno, et al., "μI/O Architecture for 0.13μm Wide-Voltage-Range System-on-a-Package (SOP) Designs," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 168-169, 2002.

 1-4244-0079-1/06/$20.00

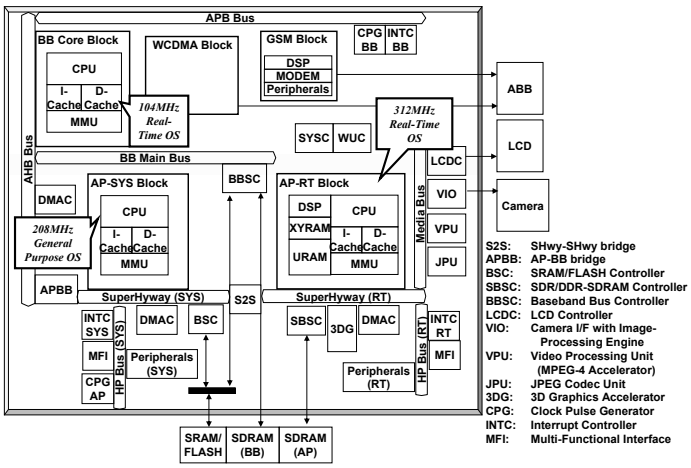


Figure 29.5.1: Processor block diagram.

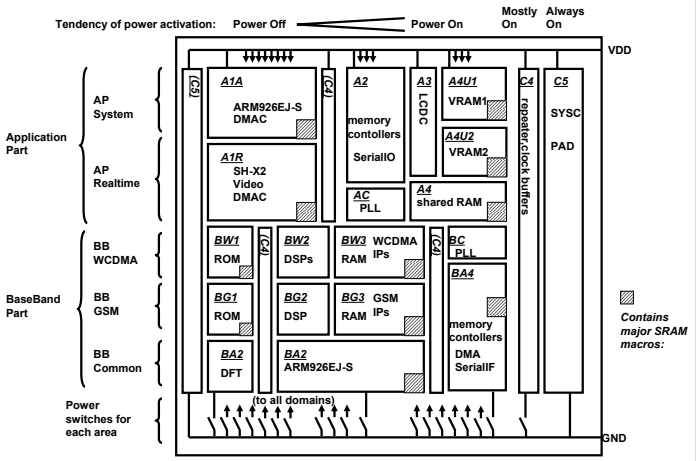
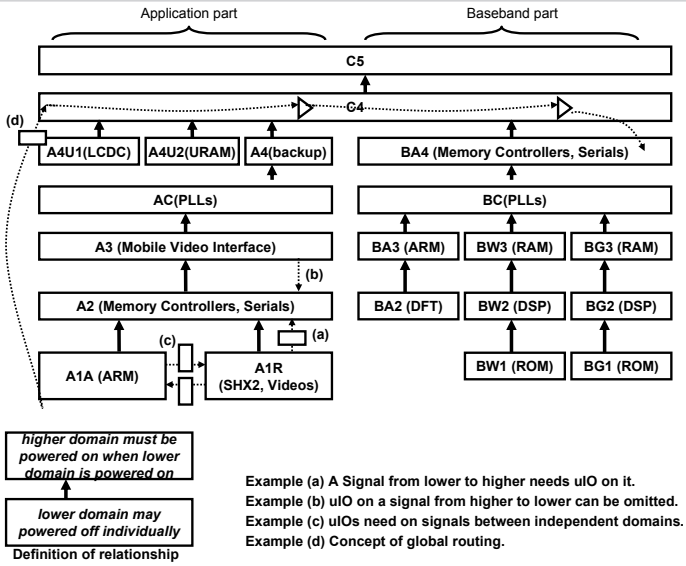


Figure 29.5.2: The Concept of Power Domains inside the chip.



Example (a) A Signal from lower to higher needs uIO on it.
Example (b) uIO on a signal from higher to lower can be omitted.
Example (c) uIOs need on signals between independent domains.
Example (d) Concept of global routing.

Figure 29.5.3: Definition of Hierarchal Relationships between Power Domains.

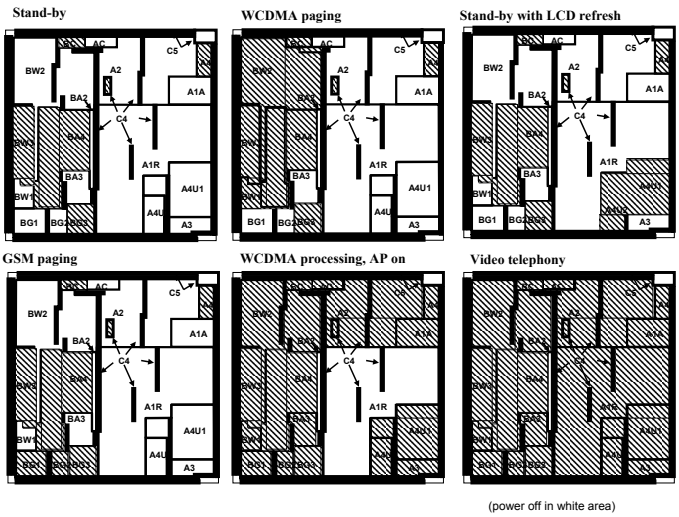


Figure 29.5.4: Example of Activating Power Domains in mobile phone scenes.

	Scene 0	Scene1	Scene 2	Scene 3
Situation	All power domains are supplied	Only telephone use	Waiting for calling	Ultra-standby
Baseband part	ON	ON	Intermittent operation	OFF
Application part	ON	OFF	Supplying Reduced Power only for Memory Domains	OFF
Leakage Current (uA @ rt, 1.2V)	849	407	299	7

Note1) Only leakage current in VDD supply is shown. Dynamic current in each scene is not included.

Note2) SRAMs are resume standby mode in scene 2.

Figure 29.5.5: Leakage current measured in several usage scenes.

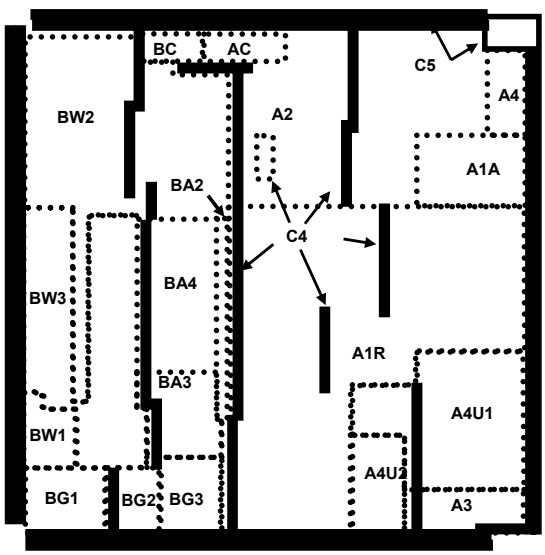


Figure 29.5.6: Power domains inside the chip.

Continued on Page 672

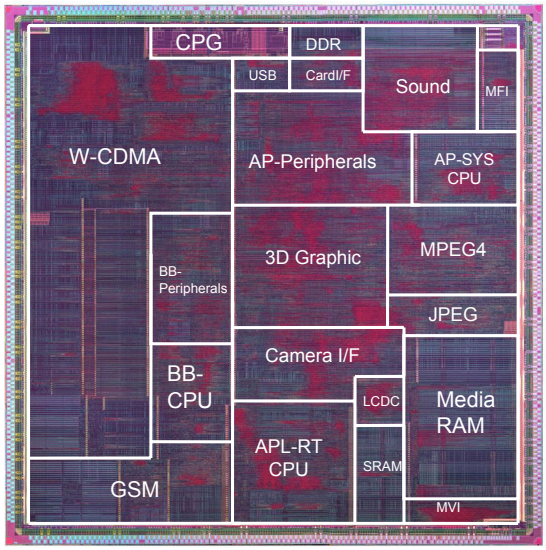


Figure 29.5.7: Die micrograph.

